ADB Technical Assistance Concept Note

Strengthening the Philippines' Semiconductor Design Capability for the Physical AI Economy

Field	Details
Country	Philippines
TA Type	Knowledge and Support Technical Assistance (KSTA)
Sector	Industry and Trade / Information and Communication Technology
Thematic Classification	Human Capital Development; Technology-Enabled Growth; Regional Equity
Estimated Cost	$4.5 million ($2.0M ADB + $2.5M co-financing)
Proposed Duration	36 months
Executing Agency	Department of Science and Technology – Philippine Council for Industry, Energy, and Emerging Technology Research and Development (DOST-PCIEERD)
Implementing Partners	SEED Foundation (to be established); Sibacus Technologies Pte. Ltd. (industry partner); University of the Philippines system; Ateneo de Manila University; De La Salle University; Mapua University

1. Background and Rationale

1.1 The Philippines' Semiconductor Paradox

The Philippines is the world's 6th largest semiconductor exporter, with annual exports exceeding $20 billion. However, this position rests almost entirely on Outsourced Semiconductor Assembly and Test (OSAT) activities — the lowest-margin segment of the semiconductor value chain (5–10% operating margins). The chips assembled and tested in Philippine facilities are designed in the United States, Taiwan, South Korea, and increasingly India and Vietnam.

The Philippines has **no domestic semiconductor design capability.** Fewer than 100 chip design engineers are estimated to work in-country (compared to 300,000+ OSAT workers). No Philippine university offers a complete chip design curriculum. No Philippine company holds meaningful semiconductor IP.

This structural gap means the Philippines captures a diminishing share of value in a growing industry. As OSAT activities face automation pressure and as competitor nations (Vietnam, Indonesia, Malaysia) invest in their own assembly capacity, the Philippines risks losing its position entirely — unless it moves up the value chain to design.

1.2 A Market-Driven Opportunity

Sibacus Technologies Pte. Ltd. (Singapore) has developed BSA-CIM (Binary Shift-Add Compute-in-Memory), a semiconductor architecture that enables artificial intelligence computation directly in resistive memory (RRAM) at substantially lower energy and cost than conventional GPU-based approaches. The technology has been validated through hardware synthesis, energy modeling, and AI model benchmarking.

Sibacus operates on the ARM Holdings business model: it designs the core IP and licenses it to product companies that build end-user devices. Sibacus has offered the Philippines **preferential (non-exclusive) licensing terms** for companies that design and manufacture products on its platform — conditional on the Philippines investing in the workforce and ecosystem to support such an industry.

This creates a time-limited opportunity: the Philippines can become the first ASEAN country to establish a Physical AI product design ecosystem on the CIM platform, attracting foreign direct investment from companies seeking preferential access to the IP, the trained workforce, and the existing OSAT infrastructure.

1.3 The Environmental-Value Circularity: From Mine to Module

The global hardware economy requires critical minerals like **nickel**, for which the Philippines is a dominant global supplier. Currently, this trade is strictly extractive: raw ore is exported with minimal local value addition, leaving local mining communities to bear the heavy environmental and social costs of extraction.

The SEED Program integrates the hardware supply chain from its source: * **Locating Processing Near Assembly:** Instead of shipping raw ore, the program advocates refining mineral resources domestically into high-value electronics packaging, substrate, and thermal management inputs. * **Environmental Rehabilitation Funding:** The substantial margins captured from this domestic value-addition and design-stage IP can be directly channeled into the environmental rehabilitation of the mining communities. * **A Just Transition for Sovereign AI:** By building a closed loop—from mining and refining to design, assembly, and community restoration—the Philippines establishes a sustainable sovereign AI model that does not exploit communities for foreign corporate gains.

1.4 Strategic Alignment

ADB Strategy 2030 (via EquaSat Missions): - Operational Priority 1 (Addressing remaining poverty and reducing inequalities): **HARVEST A-EYE** (food security and agriculture AI) and **EQUANET.ME** (broadband connectivity for underserved populations) - Operational Priority 2 (Accelerating progress in gender equality): STEM pipeline development with targeted fellowship recruitment - Operational Priority 3 (Tackling climate change): **FOREST SHIELD** (deforestation tracking) and **OCCUPY SOIL** (carbon verification) provide a direct ADB climate finance pathway. Additionally, CIM technology consumes 4–8× less energy than conventional AI chips. - Operational Priority 4 (Making cities more livable): Physical AI for smart infrastructure, flood warning, traffic management - Operational Priority 6 (Strengthening governance & regional cooperation): **OCEAN A-EYE** (maritime surveillance) and technology sovereignty through the ASEAN multi-country consortium structure (ADB's preferred model).

Philippines Country Partnership Strategy: - Human capital development and skills upgrading - Digital transformation and innovation ecosystem - Regional economic development beyond Metro Manila - Industrial competitiveness and value chain upgrading

Relevant ADB Sector Assessments: - Philippines: Education (skills mismatch in STEM) - Philippines: Industry and Trade (value chain upgrading) - Southeast Asia: Digital Economy (AI adoption readiness)

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2. Objectives and Scope

2.1 Impact

The Philippines establishes a self-sustaining semiconductor design and Physical AI product ecosystem, capturing design-stage value (30–50% margins) in addition to its existing assembly-stage position, and serving as the engineering and design backbone for the ASEAN-wide EquaSat consortium.

2.2 Outcome

By project completion (Month 36): - A trained cohort of 35+ semiconductor design engineers and researchers who will serve the EquaSat consortium - 5+ operational research and prototyping laboratories across Philippine universities - Domain-sovereign AI models (e.g., ASEAN agricultural AI, conservation AI, maritime AI) developed and deployed - 3+ Physical AI product companies incubated and operating - A national chip design curriculum adopted at 10+ engineering schools - A preferential licensing framework operational, with at least 2 FDI entrants registered

2.3 Scope

The TA supports the **SEED Program** (Sibacus Edge Ecosystem Development) — a 3-year university partnership and ecosystem development initiative to build the Philippines' first semiconductor design ecosystem on a licensable IP platform. Crucially, SEED acts as the capacity-building component that produces the engineers and ground terminal designs for **EquaSat**, the ASEAN sovereign orbital platform, with separate CAPEX structures.

Component 1: University Research and Laboratory Development ($1.8M)

Eleven research tracks across 8+ Philippine universities, covering:

Silicon and Architecture: - RRAM/CIM device characterization (UP Diliman) - CSD encoding optimization (Ateneo de Manila, UP Diliman) - RISC-V SoC design and verification (UP Diliman, Mapua, DLSU) - CIM rendering pipeline (UP Diliman, Ateneo)

Software and AI: - Noise-aware training for edge AI models (Ateneo, UP Diliman) - Residency runtime and SDK development (UP Diliman, DLSU)

Language and Market (Philippine Comparative Advantage): - Dialect translation model development for 12+ Philippine languages (UP Diliman Linguistics, UP Mindanao, MSU-IIT, University of San Carlos, UP Visayas) - Field testing and deployment research across Luzon, Visayas, and Mindanao

Hardware Integration: - PCB and module engineering (Mapua, Batangas State University)

Laboratory buildouts: - RRAM characterization laboratory at UP Diliman (probe station, parameter analyzer, environmental chamber) - FPGA prototyping laboratories (20 development boards across 4 universities) - Chip design workstations with EDA tools (5 university labs)

Component 2: SEED Fellows Program ($0.5M)

Ten named PhD fellowships in semiconductor design, computational linguistics, and edge AI — the founding generation of Philippine chip designers. Each fellowship covers tuition, living stipend (₱40,000/month), conference travel, and a 3-month research rotation with the industry partner.

Component 3: Product Design Incubator and Ecosystem Seeding ($1.5M)

- Product Design Laboratory / Incubator facility (shared workspace with IP-clean areas)
- Multidisciplinary teams (engineering + business students) designing products on the CIM platform
- Target: 5–8 product concepts prototyped; 2–3 viable companies spun out
- OEM engagement workshops with Philippine electronics manufacturers
- First reference design (S-Neo tablet/laptop) FPGA prototype build

Component 4: National Curriculum Development ($0.4M)

- Four-course chip design sequence: Intro Digital Design → RISC-V Architecture → Advanced VLSI → CIM/Emerging Architectures
- Built on open-source EDA tools (Yosys, OpenROAD, Verilator) — no license cost barrier to adoption
- Piloted at 3 universities, then rolled out to 10+ engineering schools
- Instructor training workshops for faculty from regional universities

Component 5: Program Management and Knowledge Dissemination ($0.3M)

- Steering committee operations (DOST-PCIEERD, university PIs, industry partner)

- Quarterly milestone reviews and annual portfolio assessment
- Knowledge products: research publications, open-access language datasets, policy briefs on semiconductor design ecosystem development
- Program completion workshop and lessons-learned documentation

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3. Implementation Arrangements

3.1 Executing and Implementing Agencies

Role	Entity	Responsibility
Executing Agency	DOST-PCIEERD	Overall program oversight, government coordination, co-funding disbursement
Implementing Partner	SEED Foundation	University contract management, fellowship administration, incubator operations
Industry Partner	Sibacus Technologies Pte. Ltd.	IP access (in-kind), engineering mentorship, reference design, visiting researcher hosting
University Partners	UP Diliman, Ateneo de Manila, DLSU, Mapua, UP Mindanao, MSU-IIT, UP Visayas, U San Carlos, Batangas State, TIP	Research execution, laboratory hosting, curriculum development

3.2 Governance

- **Steering Committee:** DOST-PCIEERD (chair), lead university PIs, industry partner representative, ADB observer
- **Milestone-based disbursement:** Quarterly releases against specific deliverables per track
- **Performance management:** Tracks that miss two consecutive milestones enter remediation; persistent non-performance triggers reallocation
- **Annual review:** Full portfolio assessment with go/no-go decision on each track for the subsequent year

3.3 Industry Partner Contribution (In-Kind)

Sibacus Technologies contributes in-kind resources valued at approximately $1.0–1.4M: - Open-source repository access (RTL, synthesis scripts, energy models, software stack) - Background IP research-use license for all program participants - FPGA development boards and compute credits - Visiting researcher slots (3-month rotations, Singapore-based) - Engineering mentorship and design review participation - Reference design documentation and support

This contribution is not contingent on ADB funding and does not create any equity or ownership claim by the industry partner over ADB-funded outputs.

3.4 Intellectual Property

- **ADB-funded outputs** (datasets, curriculum materials, research publications): Open access / Creative Commons
- **Co-developed technical outputs** (RTL blocks, software, algorithms): Joint ownership between university and industry partner; academic use unrestricted; commercial use licensed to industry partner
- **Student work:** Full thesis/dissertation rights retained by students
- **Industry partner background IP:** Remains industry partner property; research-use license only

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4. Cost Estimates and Financing

4.1 Cost Summary

Component	ADB (M)	Government (M)	Industry In-Kind (M)	Total (M)
1. University Research & Labs	1.0	0.5	0.3	1.8
2. SEED Fellows	0.3	0.1	0.1	0.5
3. Product Design Incubator	0.4	0.7	0.4	1.5

Component	ADB (M)	Government (M)	Industry In-Kind (M)	Total (M)
4. National Curriculum	0.2	0.1	0.1	0.4
5. Program Management	0.1	0.1	0.1	0.3
Total	**2.0**	**1.5**	**1.0**	**4.5**

4.2 ADB Financing Source Options

Source	Type	Fit	Amount
Japan Fund for Information and Communication Technology (JFICT)	Trust fund grant	ICT capacity building in DMCs — direct match	Up to $2.0M
Republic of Korea e-Asia and Knowledge Partnership Fund	Trust fund grant	Knowledge economy and technology transfer — strong fit (Korea built Samsung this way)	Up to $1.5M
Technical Assistance Special Fund (TASF)	ADB own resources	KSTA for institutional capacity building	Up to $1.0M
Clean Technology Fund	Climate finance	Energy-efficient AI hardware reducing datacenter demand	Up to $1.0M

Recommended: JFICT as primary ($1.5M) + TASF ($0.5M). Japan has strong semiconductor industry ties to the Philippines and strategic interest in ASEAN supply chain diversification.

4.3 Government Co-Financing

The government's $1.5M share can be sourced from: - DOST-PCIEERD NICER/CRADLE program funds (existing budget lines) - CHED higher education development fund (for curriculum component) - DICT digital economy allocation - DTI-BOI registered enterprise incentives (tax expenditure, not cash)

4.4 Additional Co-Financing (Non-ADB, Non-Government)

Source	Estimated Amount	Status
PhilDev Foundation	$0.9–1.4M	To be proposed
Philippine corporate partners (OSAT, conglomerates, banks)	$0.9–1.4M	Corporate social investment with SEED Ventures equity on-ramp
EDB Singapore (industry partner home government)	$0.5–1.0M	Grant to industry partner to fund in-kind contribution; creates downstream demand for Singapore-fabricated CIM modules
Private sector (OSAT companies, OEMs)	TBD	Industry engagement planned for Year 2

These additional sources are not required for the ADB TA to proceed but would scale the program's reach significantly.

> **NOTE: Pax Silica Context:** The Philippines recently joined the US-led Pax Silica semiconductor initiative, committing 4,000 acres in New Clark City as an AI-industrial hub. In July 2026, a ₱2.5 billion AI infrastructure project at the same site received **zero bidders** — because without trained designers, licensable IP, and an ecosystem of product companies, land alone is a real estate play, not a technology strategy. The SEED Program directly addresses this gap by building the human capital and product ecosystem needed to capture design-stage value. Capability is portable — trained engineers can set up in Clark, Makati, or Cebu. Empty buildings cannot. SEED creates the companies that make Pax Silica's infrastructure viable.

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5. Design and Monitoring Framework

Impact

The Philippines captures semiconductor design-stage value in the global electronics value chain.

Indicator: Philippine-originated semiconductor design IP generates measurable export revenue by 2032.

Outcome

A functional semiconductor design and Physical AI product ecosystem operates in the Philippines.

Outcome Indicator	Baseline (2026)	Target (2029)	Source
Semiconductor design engineers working in-country	<100 (est.)	135+	Program records, DOST survey
Philippine companies designing products on CIM platform	0	3+	BOI registration records
Engineering schools offering chip design curriculum	0	10+	CHED records
Open-access Philippine language AI datasets	~2 (academic)	12+	Program repository
FDI companies registered for Physical AI in PH	0	2+	BOI records

Outputs

Output	Indicator	Target
1. Research capability established	Research tracks completed with deliverables accepted	9 of 11 tracks deliver
	Laboratories operational	5 labs across 4+ universities
	Research publications	15+ journal/conference papers
2. Human capital developed	SEED Fellows enrolled and active	10 PhD fellows
	Graduate researchers trained	25+ Master's/PhD students
	Faculty trained in chip design pedagogy	20+ faculty from 10+ schools

Output	Indicator	Target
3. Ecosystem seeded	Product concepts prototyped	5–8 concepts
	Viable companies incubated	2–3 spin-outs
	OEM engagement workshops conducted	4+ workshops
4. Curriculum operational	Course sequence developed and piloted	4 courses at 3 pilot schools
	National rollout	10+ schools adopting
5. Knowledge disseminated	Language datasets published (CC license)	12+ languages
	Policy brief on semiconductor design ecosystem	1 published
	Program completion report	1 published

Activities and Milestones

Quarter	Key Milestones
Q1	TA inception; MOUs with universities; SEED Fellows selection
Q2	Research tracks launch; lab equipment procurement
Q3	First milestone review; FPGA boards distributed
Q4 (Year 1)	Mid-term review; lab buildouts complete; first research outputs
Q5	Product Design Lab opens; ecosystem teams form
Q6	FPGA prototyping begins; OEM workshops
Q7	Field testing begins (software-emulated devices)
Q8 (Year 2)	Annual review; incubator teams evaluated
Q9	Curriculum pilot at 3 schools; tape-out design review

Quarter	Key Milestones
Q10	Tape-out submitted (via Singapore fab partner)
Q11	Curriculum rollout to 10+ schools; first silicon received
Q12 (Year 3)	Program completion; spin-out companies operational; final report

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6. Risks and Mitigation

Risk	Likelihood	Impact	Mitigation
University research tracks underperform	Medium	Low	Milestone-based funding; two-strike remediation; track reallocation
RRAM foundry availability delays	Medium	Medium	Program proceeds with FPGA emulation; CIM module design validated without physical RRAM
Industry partner withdraws	Low	Medium	ADB-funded outputs (datasets, curriculum, labs) retain value independent of any single company; IP framework ensures university rights preserved
Government co-financing delayed	Medium	Low	Program components sequenced so ADB-funded activities can proceed independently; PhilDev/corporate co-financing provides buffer

Risk	Likelihood	Impact	Mitigation
Insufficient FDI interest in Pioneer License	Medium	Low	Pioneer licensing is a bonus outcome, not a program dependency; domestic ecosystem development proceeds regardless
Brain drain (trained engineers emigrate)	Medium	Medium	Competitive stipends; ecosystem companies provide local employment; the program itself creates the reason to stay

7. Precedents and Comparables

ADB and member countries have successfully funded similar technology ecosystem programs:

Program	Country	ADB Role	Outcome
Innovation and Competitiveness TA	Multiple DMCs	KSTA grants for technology parks, industry-university linkages	Functional innovation ecosystems in Vietnam, Indonesia
STEM Workforce Development	Philippines	Loan component for higher education	Improved STEM graduate employability
Digital Economy Development	Indonesia, Vietnam	Sovereign loans $100–300M	Digital infrastructure and skills
Vietnam Semiconductor HR Development	Vietnam	Knowledge partnership	Vietnam's semiconductor design workforce grew from near-zero to 5,000+ in a decade

The Philippines' proposed program is smaller in cost ($4.5M vs. typical $50–300M) and more targeted in scope, but has a stronger market-pull mechanism (specific industry partner with preferential licensing offer) than most comparable initiatives.

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8. Recommendation

ADB Management is requested to approve the provision of technical assistance not exceeding $2,000,000 from [JFICT / TASF / to be determined], on a grant basis, to the Government of the Philippines for Strengthening the Philippines' Semiconductor Design Capability for the Physical AI Economy.

Prepared in consultation with the Southeast Asia Department (SERD) and the Sustainable Development and Climate Change Department (SDCC).

Contact: [To be filled]